signal from the first clock generator, the first clock generator is configured to provide the first clock signal to the second clock generator.

[0024] According to at least one example embodiment, if the second clock generator does not request the first clock signal from the first clock generator and a clock request signal is deactivated, the first clock generator is configured to deactivate a clock response signal.

[0025] According to at least one example embodiment, the CMU further includes a manager configured to connect to the logic block according to the full handshake method. The first clock generator includes a first full handshake circuit, the second clock generator includes a second full handshake circuit, and the manager is configured to control the first full handshake circuit and the second full handshake circuit.

[0026] According to at least one example embodiment, the logic block includes an IP core, and the IP core is configured to activate a clock request signal if one of the clock signals is desired.

[0027] According to at least one example embodiment, the CMU is configured to simultaneously activate a clock response signal in response to activation of the clock request signal and provide at least one of the clock signals to the IP core.

[0028] According to at least one example embodiment, the IP core is configured to deactivate the clock request signal if the clock signals are not desired.

[0029] According to at least one example embodiment, the CMU is configured to simultaneously deactivate the clock response signal in response to deactivation of the clock request signal and deactivate the clock signals.

[0030] According to at least one example embodiment, a method of driving an SoC includes requesting, by the at least one logic block, a clock signal from the CMU according to a full handshake method. The method includes transmitting, by the CMU, the clock signal to the at least one logic block if the CMU accepts the request. The method includes performing a communication between the first clock generator and the second clock generator according to the full handshake method.

[0031] According to at least one example embodiment, the requesting includes activating, by the at least one logic block, a clock request signal if the clock signal is desired.

[0032] According to at least one example embodiment, the transmitting comprises activating, by the CMU, a clock response signal in response to activation of the clock request signal. The transmitting includes providing, by the CMU, the clock signal to the at least one logic block.

[0033] According to at least one example embodiment, the method includes deactivating, by the at least one logic block, the clock request signal if the clock signal is not desired.

[0034] According to at least one example embodiment, the method includes deactivating, by the CMU, the clock response signal in response to deactivation of the request signal, and deactivating, by the CMU, the clock signal.

[0035] According to at least one example embodiment, the method includes generating, by the first clock generator, a first clock signal, and generating, by the second clock generator, a second clock signal. The clock signal includes one of the first clock signal, the second clock signal, and a clock signal generated by combination of the first clock signal and the second clock signal.

[0036] According to at least one example embodiment, the method includes transmitting, by the first clock generator, the first clock signal to the second clock generator, and generating, by the second clock generator, the second clock signal using the first clock signal.

[0037] According to at least one example embodiment, the method includes providing, by the first clock generator, the first clock signal to the second clock generator if the second clock generator request the first clock signal from the first clock generator.

[0038] According to at least one example embodiment, the method includes deactivating, by the first clock generator, a clock response signal according to a clock request signal if the second clock generator does not request the first clock signal from the first clock generator and the clock request signal is deactivated.

[0039] According to at least one example embodiment, a device, includes a clock signal manager configured to manage at least one logic block by receiving, from the at least one logic block, a first request signal indicating a request for a first clock signal, and simultaneously sending a first acknowledgement signal and the first clock signal to the at least one logic block in response to the first request signal.

[0040] According to at least one example embodiment, the first acknowledgement signal and the first clock signal remain activated until the first request signal is deactivated by the at least one logic block.

[0041] According to at least one example embodiment, at least one clock signal is a first clock signal and a second clock signal, different from the first clock signal, and the clock signal manager includes a multiplexer configured to receive the first clock signal and the second clock signal, and transition from outputting the first clock signal to outputting the second clock signal based on a selection signal.

[0042] According to at least one example embodiment, if the selection signal indicates the transition, the clock signal manager is configured to, receive, from the at least one logic block, a second request signal indicating a request for the second clock signal, and simultaneously send a second acknowledgement signal and the second clock signal to the at least one logic block.

[0043] According to at least one example embodiment, a duration of the second acknowledgement signal overlaps a duration of the first acknowledgement signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0044] The foregoing and other features and advantages of the inventive concepts will be apparent from the more particular description of preferred embodiments of the inventive concepts, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the inventive concepts. In the drawings:

[0045] FIG. **1** is a block diagram illustrating a system-on-chip (SoC) according to at least one example embodiment of the inventive concepts;

[0046] FIG. **2** is a timing diagram according to a full handshake method;

[0047] FIG. **3** is a timing diagram for describing a problem of the related art;

[0048] FIG. **4** is a block diagram illustrating an SoC according to at least one example embodiment of the inventive concepts;